REMARKS

In the Office Action dated September 12, 2003, claims 1-25 were pending. Claims 1-25 stand rejected. In this response, no claim has been canceled. Claims 1, 9, 11, 15, 20, and 22 have been amended. In addition, portions of the drawings, title, and specification have been amended. No new matter has been added. Reconsideration of this application as amended is respectfully requested.

The title has been objected as non-descriptive. Accordingly, a new title has been proposed. Applicants respectfully request the Examiner enter the proposed title.

Portions of the drawings were objected to. In this response, Figures 2 and 4-7 have been amended. In Figure 2, term "(4) START PROGRAMMING" has been changed to "START PROGRAMMING". In Figure 4, texts have been added to the boxes requested by the Examiner. In Figure 5, box 32 has been amended to include "Spec. Prog. Mode Ccty." In Figure 6, boxes 32, 40, 62, 83, and 91 have been amended. In Figure 7, box 164 has been amended. A copy of the above proposed figures is provided in the Appendix of this response. Applicants respectfully request the Examiner accept the proposed figures.

The Examiner further requires that Figures 5 and 6 should be designated by a legend of "Prior Art". Applicants respectfully submit that Figures 5 and 6 are parts of the invention as claimed. For example, Figures 5 and 6 include, among others, the special mode circuitry 32.

Portions of the specification have been objected. In view of the foregoing amendment, it is respectfully submitted that the objections have been overcome.

Claims 9, 11, and 20 have rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. In view of the foregoing amendment, the rejections have been overcome. The support of claim 9, 11, and 20 can be found on pages 12-13 and 20 of the specification.

Claims 1-25 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending U.S. Patent Application No. 09/752,594 and claims 1-20 of copending U.S. Patent Application No. 09/749,133. Since this is a

provisional rejection, applicants respectfully submit that a terminal disclaimer will be submitted upon the allowance or patenting with one or more claims.

Claims 1-12, and 15-25 are rejected under 35 U.S.C. §103(a) as being unpatentable over the Intel Corporation Application Note AP-629 ("AP-629") or the Intel Corporation Application Note AP-678 ("AP-678"), in view of U.S. Patent No. 5,600,600 of Olivo et al. ("Olivo").

Applicants submit that claims 1-25 of the present application include limitations not disclosed or suggested by the cited references. Specifically, independent claim 1 recites:

> 1. A method comprising:
> entering a special programming mode of a memory that disables internal program verification by the memory, wherein the memory includes automation circuitry for program verification;
> programming a plurality of words into the memory during the special programming mode without the memory performing internal program verification;
> exiting the special programming mode of the memory; and
> enabling internal program verification by the memory.

(Emphasis added).

Independent claim 1 includes limitations of enabling a special programming mode of a memory by entering a special programming mode, where the enabling special programming mode disables an internal program verification by the memory. Applicants respectfully submit that the cited references, individually or in combination, fail to disclose or suggest the above limitations. Although AP-629 and AP-678 disclose a write state machine (WSM), they fail to disclose or suggest enabling a special programming mode of a memory by entering a special programming mode.

In addition, independent claim 1 includes a limitation where the enabling special programming mode disables internal program verification by the memory and a limitation of programming a plurality of words into the memory during the special programming mode without the memory performing internal program verification. Applicants respectfully submit that these limitations are also absent from the cited references, individually or in combination.

In the Office Action, the Examiner stated:

"Intel also teaches that, in order to reduce programming and testing time of a nonvolatile memory, one should consider modifying the method or program flow to perform only necessary operations (see AP-629, pages 9-10, and Figure 4). Intel further teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one can save time by not performing program verify operations (Intel (AP-629), at page 9, column 2, e.g.).

Intel (AP-678) similarly teaches that verification of each location as it is programmed or written should be eliminated from the programming routines of automated flash memories (see AP-678, at page 9, column 1, e.g., as well as page 10 and Figure 3), since program verify operations initiated by external automated test equipment (ATE) are redundant with internal program verify operations (see AP-678, at page 9, column 2)."

(9/12/2003 Office Action page 7, emphasis added).

Applicants respectfully disagree. As acknowledged by the Examiner, the external verification operations by the ATE are redundant and may be eliminated. However, these sections of AP-629 and AP-678 do not read on the limitations of claim 1 set forth above, where the enabling special programming mode disables internal program verification by the memory and programming a plurality of words into the memory during the special programming mode without the memory performing internal program verification. Both AP-629 and AP-678 disclose or suggest eliminating the external verification operations. That disclosure teaches away from the amended claim 1. Specifically, the AP-629 discloses the following:

"The flash memory internal Write State Machine (WSM) automatically verifies data written to the memory. Program verify operations initiated by the ATE are redundant with flash memory internal program verify operations. You can save time by not performing program verify operations with the ATE."

(AP-629 page 9, col. 2, emphasis added).

That is, the AP-629 clearly discloses or suggests eliminating the external verification operations, rather than the internal verification operations as claimed by claim.

The Examiner states that:

"Olivo discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (see column 1, lines 26-62; column 2, lines 9-31; and column 4, lines 7-12 and 32-36)."

(9/12/2003 Office Action, pages 7-8, emphasis added).

Applicants respectfully disagree. The section of Olivo relied on by the Examiner does not disclose or suggest disabling internal verification operations during the "special" programming mode. Specifically, Olivo states:

> "Consequently, having excluding the internal state machine 11, the addresses can be used freely and, using the above listed control signals with their new meaning, the desired cells can be programmed and their correctness can be verified."

(Olivo col. 4, lines 32-36, emphasis added).

Olivo further states:

> "Verification is performed by a comparison of the values present after memory programming with the correct ones supplied through the data bus 3. The signal CEN also returns to a low logic value Vil and the circuit is ready to perform a new test or return to normal operation.
>
> The test method in accordance with the present invention has the following advantages: The memory matrix test can be performed in a manner fully independent of control unit operation. The duration of the programming pulse and that of the verification phase are not bound to the internal time base and can thus be selected at will. The sequence of performance of the actual test is compatible with that used for testing EPROM memories of the known art and thus permits use of the same circuitry equipment for its performance."

(Olivo col. 4, line 63 to col. 5, line 10, emphasis added).

Thus, applicants respectfully submit that Olivo fails to disclose or suggest the limitations of the amended claim 1 set forth above.

The AP-629 or AP-678 does not teach or suggest a combination with Olivo, and Olivo does not teach or suggest a combination with the AP-629 or AP-678. It would be impermissible hindsight, based on applicants' own disclosure, to combine AP-629 or AP-678 and Olivo.

Even if Olivo and AP-620 or AP-678 were combined, such a combination would still lack the limitations referred to by claim 1, which are set forth above. Therefore, for the reasons set forth above, independent claim 1 is patentable over the cited references.

Similarly, independent claims 15 and 22 include limitations similar to those referred to by claim 1. Thus, for reasons similar to those discussed above, it is respectfully submitted that independent claims 15 and 22 are patentable over the cited references.

Given that claims 2-14, 16-21, and 23-25 depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that claims 2-14, 16-21, and 23-25 are patentable over the cited references.

In view of the foregoing, applicants respectfully submit that applicable rejections and objections have been overcome.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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